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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G08G 1/017, G06K 9/46, 9/36, 9/60 — A1

(11) International Publication Number: WO 94/28527

(43) International Publication Date: 8 December 1994 (08.12.94)

(21) International Application Number: PCT/AU94/00260

(22) International Filing Date: 23 May 1994 (23.05.94)

(30) Priority Data:
PL 8944 24 May 1993 (24.05.93) AU

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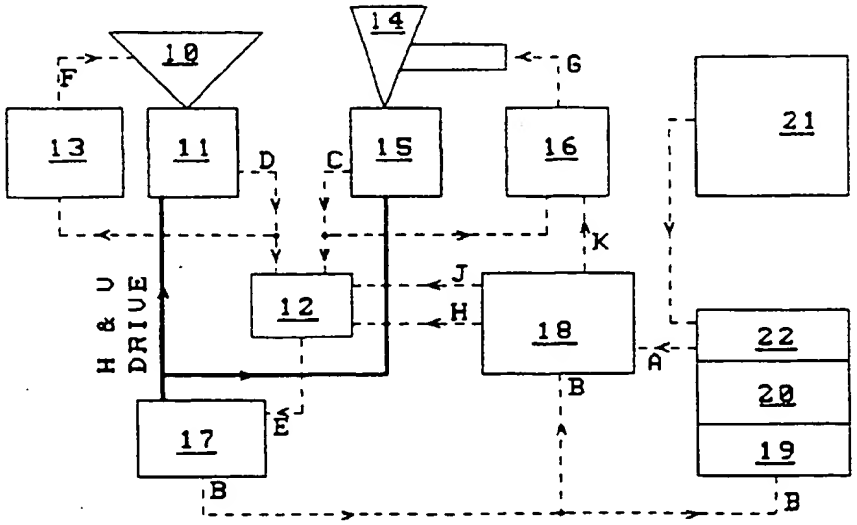
(81) Designated States: AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, ES, FI, GB, GE, HU, JP, KG, KP, KR, KZ, LK, LU, LV, MD, MG, MN, MW, NL, NO, NZ, PL, PT, RO, RU, SD, SE, SI, SK, TJ, TT, UA, US, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: IMAGE STORAGE SYSTEM FOR VEHICLE IDENTIFICATION



(57) Abstract

An image storage system suitable for use with devices for detecting/recording overspeeding vehicles. The system includes at least one image sensor (11, 15, 53, 55) for generating data representing an image applied to the sensor. The system includes means for applying a first image (10, 54) to the sensor (11, 53) for generating first data representing at least relatively coarse features in the first image, and means for applying a second image (14, 56) including an enlarged portion of the first image to the sensor (15, 55) for generating second data representing at least relatively fine features in the first image. The second data representing relatively fine features has a set level of definition. The first data representing relatively coarse features has a level of definition which is below the set level. The quantity of data is thereby reduced for storage purposes. A data storage system including a frame grabber (19) and digital computer (20) having a hard disk is also disclosed.

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IMAGE STORAGE SYSTEM FOR VEHICLE IDENTIFICATION

The present invention relates to an image storage system. In particular the present invention relates to an image storage system suitable for use in connection with devices for detecting/recording overspeeding vehicles known generically as "speed cameras". Nevertheless, it is to be appreciated that it is not thereby limited to such applications.

Prior art devices used for detecting/recording vehicles which exceed speed limits are based on conventional photographic techniques using films coated with light sensitive emulsions which must be exposed, developed and stored in film or hard copy format. This is not only a costly procedure but creates bulky records in the form of rolls of exposed film which are cumbersome to store and handle. Because a typical roll of film may contain hundreds of traffic infringements or violations, access to a specific infringement or violation in such a roll of film is a time consuming exercise.

Using conventional techniques, the image of a vehicle from which the license plate can be read and which shows the mandatory surrounding roadway and vehicles needs to have a relatively high resolution or definition. To achieve such definition or resolution the image typically needs to be made up of at least about 1.4 million picture elements or pixels, each able to represent one of about 64 shades of grey. A file generated from such an image occupies over 1.4M Bytes of storage space. Although state of the art file compression techniques can reduce this by up to 60% (570 K Bytes), the processing time involved reduces the overall operating speed considerably.

An object of the present invention is to provide an image storage system which at least alleviates the disadvantage of the prior art.

The system of the present invention may reduce the size of an uncompressed file or record by a factor of at least 10 or more, yet still provide similar resolution or definition in a relevant area or portion of the record. The system of the present invention may achieve a

reduction in file or record size by capturing two images of a vehicle to be recorded, each having a relatively low resolution. One image may be captured using a relatively long focal length or telephoto lens. The telephoto image of the vehicle may show relatively fine or detailed features such as a vehicle license plate, vehicle make and model and in some cases facial features of the occupants. A further image may be captured using a relatively wide angle lens. The wide angle image may show relatively coarse or less detailed features such as the infringing vehicle in relation to the surrounding roadway and other vehicles. The infringing vehicle may still be clearly recognizable in the wide angle image.

The two images may be captured via at least one image sensitive device or sensor such as a CCD (charge coupled device) array or vidicon tube. The or each image sensor may have relatively low resolution or definiton. Nevertheless, higher resolution or definition image sensors may be used since it is always possible to reduce resolution or definition by discarding superfluous or unwanted image data prior to recording the data.

In one form, the or each image sensor may be capable of generating data representing an image containing at least about 50,000 picture elements or pixels, with each element or pixel being able to represent one of about 64 shades of grey. A record or file generated from such data may occupy no more than about 50 KBytes of storage space. The record or file representing two such images for each vehicle infringement may occupy about 100 K Bytes of storage space whilst still containing relevant infringement data. This is less than one tenth of the size of a comparable single picture system without compression techniques.

It is to be appreciated that no matter what is the final resolution or definition of an image required to be stored, the principles of the present invention may be applied to provide considerable savings in record or file size and operating speed over prior art approaches.

According to one aspect of the present invention there is provided apparatus for use with an image storage

system, said apparatus including at least one sensor for generating data representing an image applied to said sensor; means for applying a first image to said at least one sensor for generating first data representing at least relatively coarse features in said first image; means for applying a second image comprising an enlarged portion of said first image to said at least one sensor for generating second data representing at least relatively fine features in said first image, said second data representing said relatively fine features with a set level of definition and said first data representing said relatively coarse features with a level of definition which is below said set level, whereby reducing the quantity of said data for storage purposes.

According to a further aspect of the present invention there is provided an image storage system including:

at least one image sensor for generating data representing an image applied to said sensor;

means for applying a first image to said at least one sensor for generating first data representing at least relatively coarse features in said first image;

means for applying a second image including an enlarged portion of said first image to said at least one sensor for generating second data representing at least relatively fine features in said first image;

said second data representing said relatively fine features with a set level of definition and said first data representing said relatively coarse features with a level of definition which is below said set level; and

means for storing said data.

The means for applying the first image may comprise a wide angle lens having a focal length of approximately 50mm. The means for applying the second image may comprise a telephoto lens having a focal length of approximately 210 mm. The two lenses may be associated with a single image sensor. The image sensor may be fixed and the lenses may be movable or the lenses may be fixed and the sensor may be movable. Alternatively, a single zoom lens (eg. 50-210mm) may be used in place of the two

lenses. Preferably each lens is associated with a respective image sensor. The address lines of the respective image sensors may be driven in parallel via common driving circuits. In one form the apparatus may include a self contained board video camera. Two image sensors may be used with a single board video camera. The horizontal and vertical address lines of each image sensor may be driven in parallel via the board video camera.

The first and second images may be generated simultaneously or sequentially. Where the first and second images are generated sequentially, means such as a video switch or the like may be used to switch between the outputs of the respective image sensors.

The respective outputs may be processed in the usual way via the board video camera to provide a composite video or luminance signal at its output. The composite video or luminance output signal may be connected to a frame grabber circuit. The frame grabber circuit may include a memory. The frame grabber circuit may also include an analog to digital converter. The frame grabber circuit may be adapted to store one field (odd or even) from the composite video or luminance signal. Where the resolution of the composite or luminance video signal is greater than about 100,000 picture elements or pixels per frame (2 fields), the frame grabber circuit may be arranged to limit the quantity of data stored from each field such that the resolution of the stored field is limited to about 50,000 picture elements or pixels. This may ensure that the size or volume of the record or file for each field is of a manageable size. The frame grabber circuit preferably is adapted to store the composite video signal in monochrome (luminance) to minimize the quantity of data stored from each field.

According to a further feature of the present invention the frame grabber circuit may store a sample of the first and/or second image in color (luminance plus chrominance). The color sample may be taken from a relatively small relevant portion or area of the first and/or second image, such as a portion showing the color of an infringing vehicle, and this may be stored together

with the monochrome image. When the image is reviewed the portion or area from which the color was sampled may appear in true color against a monochrome background. This technique may provide additional means of vehicle identification with minimum increase in image file size. A change from monochrome to colour usually results in a threefold increase in file size with proportional decrease in overall operating speed. However the increase in file size is limited to the sampled area. Thus if the sampled area is 1% of the overall image area a 2% increase in overall file size can be expected.

The frame grabber circuit may transfer its data to any suitable storage medium such as a computer hard disk, static RAM or the like. The data may be transferred to storage medium with other infringement related information such as details of location, user ID, speed zone together with infringing vehicle speed, distance, time and date etc.

The associated computer may be programmed to control operation of the apparatus of the present invention. Alternatively a dedicated microprocessor based controller may be used. The apparatus may be triggered via any suitable speed/distance measuring device such as a radar based speed detector or preferably a laser based speed detector such as a model LTI 20-20 manufactured by Laser Technology Inc. of Englewood, Colorado USA.

The speed detecting/recording apparatus may be stationary relative to the roadway or it may be mounted in a moving patrol vehicle. Where the apparatus is mounted in a moving patrol vehicle means such as a summer device may be provided to determine absolute speed of a target vehicle from the relative speed of that vehicle and the patrol vehicle. The relative speed of the target vehicle may be determined by a speed detector mounted in the patrol vehicle. The speed of the patrol vehicle may be determined via a speedometer or tachometer in the patrol vehicle.

Preferred embodiments of the present invention will now be described with reference to the accompanying drawings wherein:-

Fig. 1 shows a block diagram of a speed camera

incorporating an image storage system according to one embodiment of the present invention;

Fig. 2 shows a block diagram of the interface and logic control module;

Fig. 3 shows a schematic diagram of one embodiment of the present invention;

Fig. 4 shows a lens iris drive circuit associated with the embodiment of Fig. 3;

Fig. 5 shows a block diagram of a speed camera incorporating an imaging storage system according to a further embodiment of the present invention;

Fig. 6 shows a flow chart of one form of operation program which is employed for controlling an image storage system;

Fig. 7 shows a schematic diagram of a further embodiment of the present invention;

Fig. 8 shows a schematic diagram of a logic module included in Fig. 7; and

Fig. 9 shows a lens iris drive circuit associated with the embodiment of Fig. 7.

Referring to Fig. 1 the system includes a wide angle lens 10 and associated CCD image sensor 11. The output (D) of image sensor 11 is connected to a first input of analog video switch 12 and to an automatic exposure interface 13 associated with wide angle lens 10. Lens 10 comprises a 50mm galvanometer type auto - iris device such as a COSMICAR type MCA5018APC. Auto exposure interface 13 amplifies and buffers signals from sensor 11 and supplies them to the galvanometer type auto iris associated with lens 10.

The system includes a telephoto lens 14 and associated CCD image sensor 15. The output (C) from image sensor 15 is connected to a second input of analog video switch 12 and to an automatic exposure interface 16. Since compact telephoto type auto-iris lenses are not readily available, this was developed by modifying a 210mm focal length compact zoom lens (Sigma type) designed for a 35mm SLR camera. The lens preferably is suitable for use in the infrared region for night time operation. The zoom lens may be fixed at maximum focal length and the iris

detent spring and ball associated with the ring removed. A ring gear may be fitted to the iris ring and the lens fitted to an adapter to allow mounting of CCD sensor 15. The adapter may also include a mounting for a DC micro-servo motor (Minimotor SA type 1016) which may drive the lens iris ring via a small spur gear.

Interface 16 may be adapted to sample a horizontal scan line, from image sensor 15 eg. about half way down the image. This sample may be converted to a suitable level and applied to drive the auto iris servo motor associated with telephoto lens 14. This arrangement may provide closed loop feedback to automatically control exposure of image sensor 15.

The system includes a self contained video camera module 17 such as a TMC-7 series CCD board camera manufactured by PULNIX. Video camera module 17 includes horizontal and vertical driving circuits for CCD sensors 11 and 15, timing and synch generators and a video amplifier for producing a composite video output signal (B). Camera module 17 may also include an auto iris control output for use with standard type auto iris lenses. CCD sensors 11 and 15 are connected to the horizontal and vertical driving circuits on camera module 17 in parallel.

Video switch 12 is adapted to alternately connect the output (D) of sensor 11 or output (C) of sensor 15 to the CCD sensor input (E) of camera module 17 under control of interface and logic control module 18. The latter is described in more detail with reference to Fig. 2.

The composite video output signal (B) is connected to interface and logic control module 18 and to frame grabber 19 associated with an IBM compatible personal computer (PC) 20. Frame grabber 19 may comprise a PC frame grabber card such as a FG 302 TV frame grabber PCB. Frame grabber 19 may occupy a single slot in PC 20. Its function is to digitize and store one field of a monochrome or color TV signal with (approximately) 256 x 256 pixel resolution (7 bits grey scale resolution per pixel) and to transfer the image data to the computer memory (RAM) in a sequence of DMA cycles. A TV monitor

output of the stored image is not provided on the FG 302. However images may be displayed on a monitor (eg. LCD) associated with PC 20.

The system is triggered via a trigger device 21 such as a laser based speed detector (eg. LTI 20-20) connected to PC 20 via an RS 232 port 22.

Referring to Fig. 2, interface and logic control module 18 comprises a synch separator 23 such as an LM 1881. Synch separator 23 receives at its input a composite video signal (B) from camera module 17 and provides at its output an odd/even field signal having a falling edge at the end of an odd field and a rising edge at the end of an even field. The odd/even field signal is connected to one input of RS bistable latch 24. Synch separator 23 also provides at its output a vertical synch pulse (K) to auto exposure interface 16. A control signal (A) to latch 24 is provided from RS 232 port 22 of PC 20. The Q and $\overline{Q}$ outputs of latch 24 are adapted to control the position of analog video switch 12 which alternately switches the signal (C) from sensor 15 or the signal (D) from sensor 11 to the CCD input (E) of camera module 17.

Referring to Fig. 3, the control signal (A) from PC 20 is connected to one input of latch 41A and B (4011) via diode D3 and resistor R1. Control signal (A) switches latch 41A and B causing a change in output signals (H and J) to video multiplexer switch IC6A and C (4066). This causes the input signal (E) to camera module 17 to change from, say, output (D) from wide angle sensor 11 to output (C) from telephoto sensor 15. Lines (C), (D) and (E) are single lines. All other lines between sensors 11, 15 and camera module 17 are connected in parallel. Control signal (A) also instructs frame grabber 19 to store the next odd field from composite input signal (B). Following this, PC 20 carries out a Direct Memory Access (DMA) transfer of image data from frame grabber 19 to Random Access Memory (RAM).

A further control signal (A) returns video multiplexer switch IC 6A and C to its previous state causing the output (D) from wide angle sensor 11 to be connected to the input (E) to camera module 17. Control

signal (A) again instructs frame grabber 19 to store the next odd field. Image data from wide angle sensor 11 is again transferred to RAM via DMA. Details of location, user ID and speed zone are entered into PC 20 during set-up and this data, together with the infringing vehicle speed, distance, time and date may be embedded into a single file with the two images of an infringing vehicle. This complete file, occupying about 102 KBytes is stored on the hard disk of PC 20.

Auto exposure interface 13 comprises a converter/driver made up of transistor M1, resistors R7, R8, R11 and R13 and capacitors C6, C8 and C16. An output (D) from wide angle sensor 11 is applied to the base of transistor M1 via capacitor C16 and resistor R11. The output (F) of the converter/driver is available at capacitor C8 and is applied to the auto iris drive of wide angle lens 10.

Night time operation may be enabled by a 2mS duration signal from monostable IC3A (4528) which is synchronized to the effective camera "shutter open" period via latch 41A and B. This signal may be transmitted to a large array of infra-red diodes placed at a distance at which the speed detector or trigger (eg. LT1 20/20) is set to operate. By this means an infringing vehicle may always be in an optimum flash illumination zone and focus. The infra-red filter normally fitted to the CCD camera may be removed. For day time operation the depth of field of the lenses preferably are arranged to produce well focused images in the range 60-100m. For night time operation, the speed detector/trigger may be placed in automatic mode where a target vehicle distance falls within a defined window before a reading is taken. This distance may be chosen to be optimum for lens focus and infra-red illumination and may be adjustable. For night time operation at least, it is preferable that frame grabber 19 stores a frame from output (C) from telephoto image sensor 15 before it stores a frame from output (D) from wide angle image sensor 11.

Referring to Fig. 4 an output (C) from telephoto sensor 15 is routed via diode D6 to DC amplifier IC5

(LM108). The output from DC amplifier IC5 is applied to the input of sample and hold amplifier IC6 (LF 398). The command to sample is obtained from sample time monostable IC4B (4528) set to 52μS (duration of one line). Monostable IC4B is triggered via monostable IC4A (4528) approximately 10mS (duration of half a frame) after each vertical sync pulse provided by sync separator IC2 (LM1881) (refer Fig. 3). The sample voltage is then proportional to the brightness of a single horizontal scan line approximately half way down a field. Samples representing lines or parts of lines elsewhere in a field may be chosen by changing the timing of monostables IC4A and/or IC4B.

The sample voltage is applied to servo amplifier IC7 (L272M) comprising dual power op amps which drive the auto iris servo associated with telephoto lens 14. The iris servo is isolated from low out-of-range signals by means of microswitch S1, mounted on the lens body. Steering diodes D4 and D5 provide individual direction control.

Referring to Figs. 5 and 6, actuation of the trigger device (eg. laser speed-gun) produces an output which passes via interfaces 50, 51 to an associated computer (not shown) and is examined by an operation program (refer Fig. 6) stored in the computer. The program examines the output of the trigger device and decides whether the data is valid according to criteria of the trigger device. If so, the program compares the captured speed of a target vehicle with a pre-set limit. If this has been exceeded a high state signal is sent from the computer to logic module 52 via interface 51. Logic module 52 controls, inter alia, switching to camera module 57, outputs (CCD OUT) from CCD sensor 53 associated wide angle lens 54, and from CCD sensor 55 associated with telephoto lens 56, respectively. The high state signal instructs logic module 52 to switch to camera module 57 the output from telephoto sensor 55. The operation program then instructs the computer to store image data from telephoto sensor 55.

A low state signal is then sent from the computer to logic module 52. The low state signal instructs logic module 52 to switch to camera module 57 the output from

wide angle sensor 53. The operation program then instructs the computer to store image data from wide angle sensor 53. The image data is then transferred into memory, a unique file name is created and time, date, vehicle speed and distance are appended to the file which is then stored onto hard disk. The computer is then ready to accept a new infringement.

Logic module 52 also controls an auto iris servo motor (not shown) associated with wide angle lens 54, and via drive signals applied to iris module 58, controls auto iris servo motor 59 associated with telephoto lens 56.

Although the horizonal and vertical drive between camera module 57 and sensors 53, 55 (H & V drive) is shown as a single line, it represents 12 horizonal and vertical lines. The electronic shutter speed of camera module 57 is fixed internally to 1/500 sec. Camera module 57 provides both a composite color output and a Y/C (luminance/chrominance) output. The luminance output is fed to a frame grabber associated with the computer via interface 51. The luminance output is preferred since encoded color information substantially degrades a monochrome image. The "Y" signal also contains all of the synchronizing signals necessary to drive various parts in the circuit.

A composite color signal is provided as an output to the system to assist in setting up and for continuous monitoring of the video signal if required. Images so produced appear as normal color video. As a violation or infringement is recorded, the output switches from the wide angle lens to the telephoto lens for two frames and then back again, providing a useful video tape back up if required.

Referring to Fig. 7, a high level signal sent from the associated computer is routed to the circuit via port J7. Possible voltage spikes are limited via zener diode Z1, while resistor R1 limits current flow into Z1 and resistor R2 provides a DC current path to ground from input pin 4 of IC2 which comprises a programmable logic device (PLD) such as an EP910J.

Referring to Fig. 8 which shows the circuit embedded in PLD IC2, input pin 4 is applied to macrocell ICZ2 which has no function save to transmit identical signals from input to output. This signal is additionally routed via macrocell ICZ3 to output pin 11.

Referring again to Fig. 7, the output from pin 11 of IC2 is fed to the bases of NPN transistors N1, N2 via resistors R18, R19 respectively, which serve to limit base current. Relays R16, R17 form the collector loads for transistor N1, N2 respectively while diodes D7, D8 clip any reverse voltage spikes caused by the inductance of relay coils associated with relays R16, R17.

Relays R16, R17 switch port J5 associated with the input to camera module 57 (Fig. 5), between port J4 associated with the output of telephoto CCD sensor 55, and port J6 associated with the output of wide angle CCD sensor 53. Resistors R3 and R4 provide impedance matching for CCD sensors 55 and 53 respectively. Relays R16, R17 each comprises a double pole relay to optimize isolation between signals from the wide angle and telephoto sensors 55, 53 respectively. Capacitors C5 and C6 minimize cross talk between the outputs of the respective sensors while resistor R5 provides a suitable input impedance to camera module 57.

Initially with a low state signal being sent via port J7 from the computer, both transistors N1, N2 are turned off, neither relay R16, R7 is energized and the output from wide angle sensor 53 is routed from port J6 through a normally closed contact associated with pin 4 of relay R17 across a moving contact set from pins 2 to 7 of relay R17 and out on pin 5 of relay R17 where it is routed to the input of camera module 57 via port J5. Capacitor C6 has a negligible effect on the video signal.

Signals from telephoto sensor 55 are routed from port J4 via pin 3 to pin 2 of relay R16. Radiation of this signal is minimized via capacitor C6. When the computer outputs a signal via port J7 to change from telephoto sensor 55 to wide angle sensor 53, a high level signal is applied to the bases of transistors N1, N2. This causes the collector currents so produced to energize

both relays R16, R17. The signal produced by telephoto sensor 55 is routed via port J4, then transferred from pin 3 of relay R16 via pins 2 and 7 to pin 6 which is connected to the input of camera module 57 via port J5. Wide angle sensor 53 is disconnected via pin 4 of relay R17 and radiation of this signal is minimized by capacitor C6.

The computer then instructs the frame grabber to freeze a frame taken via telephoto sensor 55. This is followed by a command to transfer the contents of this stored frame into memory. On completion of this action the computer issues a further signal via port J7 to change the signal path to the original route. Port J7 is pulled low by the computer allowing both transistors N1, N2 to be turned off. Both relays R16, R17 are released. The signal from telephoto sensor 55 via port J4 is transferred from pin 3 of relay R16 to pin 2 disconnecting it from the input of camera module 57. The signal from wide angle sensor 53 is connected to pin 4 of relay R17 and via pin 2 to pin 7 then to pin 5 of relay R17 and to port J5.

The computer waits for the next odd field, then issues a further signal to the frame grabber to freeze the second image taken via wide angle sensor 53. This image data is transferred into memory, a unique file name is created and time, date, vehicle speed and distance one appended to the file which is then stored onto hard disk. The computer is then ready to accept a new infringement.

Automatic aperture control of the wide angle lens auto iris is provided by the signal from wide angle sensor 53 via port J6. Capacitor C1 excludes unwanted lower frequencies from the signal while resistors R6, R7 form a voltage divider to suitably proportion the signal. Capacitor C2 prevents dc interaction between the base of transistor T1 and the incoming signal. Resistors R8, R9 provide a collector load and appropriate forward bias for transistor T1. The dc component of the amplified signal is filtered via capacitor C3 and the resulting signal is applied to drive the wide angle auto iris via port J2. Electrolytic capacitor E1 provides decoupling of the power supply line.

Automatic aperture control of the auto iris associated with the telephoto lens is provided by means of a separate sampling circuit. Composite video signals are fed to port J8 from camera module 57. The composite video signals are applied to pin 2 of synch separator IC5 (LM 1881) via dc blocking capacitor C10. When provided with composite video signals, IC5 provides outputs of odd/even fields at pin 7, vertical synch at pin 3, horizontal synch at pin 15 and composite synch which is not used in this application. Capacitor C9 and resistor R28 provide the correct time constant for the internal frame integrator of IC5. A negative going vertical synch pulse from pin 3 of IC5 is applied to pin 3 of PLD IC2, while horizontal synch pulses from pin 5 of IC5 are applied to pin 19 of IC2.

Referring to Fig. 8, input pin 3 is applied to pin 1 of two input NAND latch IC1A. This sets output pin 3 of latch IC1A high allowing horizontal synch pulses from pin 5 of IC5 to clock binary counters ICB and ICC via input pin 19 and gate ICH. When a binary count of 159 is decoded by ICE, ICF and ICG, this high level is output from ICG for the 64µS duration of horizontal line 159 via macrocell ICK2 to output pin 12 of IC2. Counters ICB and ICC continue counting until a count of 255 is reached when the ripple-carry out (RCO) pin 15 of ICC goes high. This signal is inverted via ICD and applied to pin 2 of IC1A which sets pin 3 low and prevents clock pulses from reaching counters ICB and ICC thus leaving the counters in this state. This provides timing for a sample signal from a horizontal line approximately half way down the image.

Referring to Fig. 7, this sample signal is outputted on pin 12 of IC2 via diode D6 to pin 2 of port J1. Diode D6 prevents accidental voltages appearing at pin 2 of port J1 from destroying IC2. Resistor R15 provides some degree of static protection for pin 12 of IC2 when left disconnected for servicing.

Referring to Fig. 9, the sample signal so generated is fed from pin 2 of port J1 to pin 8 of IC2 (LF 398), a sample and hold amplifier. This allows sample and hold amplifier IC2 to take a sample of the voltage produced by telephoto sensor 55 which is a close approximation of the

average light level across the entire 159th horizontal line. The analog input to pin 3 of sample and hold amplifier IC2 is provided from telephoto sensor 55 via pin 3 of port J1 and is scaled to an appropriate level by a voltage divider comprising resistors R12, R13. The same signal is applied to pin 3 of IC1 (LF 398), a second sample and hold amplifier. The logic input (pin 8) of sample and hold amplifier IC1 is provided by PNP transistor T1. Transistor T1 forms an inverting amplifier which is gated on during the black level period by the 'horizontal sync' pulses decoded by IC5 of Fig. 7. These pulses are labelled 'burst' as they are intended to provide timing for the color burst of a composite video signal. However, they conveniently occur at black level when monochrome video is used. Capacitor C7 blocks the dc component of the "horizontal synch". Resistor R19 holds transistor T1 in the 'off' state except during the negative going "horizontal sync" pulses applied to the base which turn it on for the duration of each pulse. Resistor R18 provides the collector load for transistor T1. Positive going pulses appearing at the collector of T1 are applied to the logic input (pin 8) of IC1 and provide a 'black level' reference at pin 5 of IC1.

Electrolytic capacitor E4 provides decoupling of the power supply line. Capacitor C3 provides requisite storage for the black level sample, while capacitor C6 provides requisite storage of the 159th line of the CCD sensor output. Suitable offset reference for IC1 is provided by a voltage divider comprising resistors R9, R10. Output signals obtained at respective pins 5 of amplifiers IC1, IC2 are applied to the inputs of differential amplifier IC3 (LM108). The dc gain of IC3 is set by resistors R4, R5, R3 and R11. Frequency compensation is provided by capacitor C1 while frequency response is limited to an extremely low level by capacitor C2. Further, limiting and smoothing of the signal is provided by resistor R6 and electrolytic capacitor E1.

IC4 (L272M) contains two operational amplifiers and because of its output drive capability is used as a driver for the telephoto lens iris servo-motor. The error signal

provided by IC3 is fed to one inverting input (pin 8) of IC4 via resistor R31. Resistors R31, R14 control the dc gain of this driver amplifier. Resistor R7, trimpot P1 and resistor R8 form a voltage divider with an adjustable operating point. Trimpot P1 is used to set a reference signal which is associated with the appropriate light level reaching telephoto sensor 55. Electrolytic capacitor E7 stabilizes the reference signal against minor noise and spikes. This reference signal is applied to a non-inverting input (pin 7) of one amplifier of IC4.

The second amplifier of IC4 is used to provide a high current, voltage centre point allowing bi-directional operation of the telephoto iris DC servo motor connected via port J11. A reference voltage for this second amplifier is provided at pin 6 of IC4 from a voltage divider comprising resistors R16, R17 with unwanted noise being filtered by electrolytic capacitor E6. A small amount of positive feedback is applied to the system via resistor R26.

The error drive signal is applied to the telephoto iris drive motor connected between pins 1 and 3 of IC4 via diode D6. Diodes D6, D7 are included to prevent stalling of the servo motor when maximum aperture is reached. When this happens, the contacts of limit switch J12 open and current can only flow in the direction necessary to close the aperture. During normal operation the contacts of limit switch J12 are closed and diodes D6, D7 are in parallel and allow bi-directional operation of the iris servo motor. It was found unnecessary to include a second limit switch at maximum lens aperture as maximum light levels do not reach this point. Capacitor C4 and resistor R15 prevent spurious oscillations in this section of the circuit.

Flash synchronization is provided by means of a 2mS synch pulse generated for each picture by the system. Referring to Fig. 8, it may be seen that for every edge applied at input pin 4, a negative going spike, the duration of which is equal to the total transfer time of gates ICZ2 and ICZ will be formed at the output (pin 3) of XOR gate ICY.

Input pin 5 is connected to odd/even field pin 7 of IC5 in Fig. 7 and goes high at the beginning of an odd field. With pin 1 of ICU normally high, pin 3 must be low. At the beginning of the next odd field (which is the only time the frame grabber can be instructed to store an image) the odd/even field signal at pin 2 of ICU produces a negative going spike at the output (pin 3) of ICX, the duration of which is equal to the transfer time of gates ICV and ICW.

This spike coincides with the start of an image to be captured and is applied to pin 1 of ICK. This action sets pin 3 of ICK high, allowing 'horizontal synch' pulses through gate ICJ to clock counters ICL1 and ICL2. The binary outputs of these counters are decoded by ICM at a count of 31. This number of 64µS pulses produces a period of 1984µS. The output of ICM goes low when 31 is decoded. This low going signal is applied to input pin 2 of ICK. This action sets output pin 3 low stopping further 'horizontal synch' pulses from clocking the counters. The positive going edge on the input of ICN generates a negative going spike at the output of ICQ which is applied to the "clear" inputs of counters ICL1 and ICL2, resetting these counters to zero. The duration of the "strobe" signal at ICK pin 3 is approximately 2mS and is output at gate ICK3 and output pin 9.

Referring to Fig. 7, the strobe signal at pin 9 of IC2 (labelled 2MS) goes high for approximately 2mS and is applied to the base of NPN transistor T via resistor R14. Transistor T is configured as an emitter follower with load provided via resistor R27. This buffered signal is taken from the emitter load and outputted at port J9.

Power to the circuit is provided via IC regulators L1 and L2 shown in Fig. 7. IC regulator L1 (LM2948) is configured as a 10 volt regulator. A 12 volt supply is applied to input pin 1 with some smoothing carried out by electrolytic capacitor E7. Diode D2 minimizes damage by reverse voltage at the input. Resistors R10, R11 form a reference voltage for regulator L1, while electrolytic capacitor E3 minimizes noise and ensures stability of this signal. Electrolytic capacitor E2 provides further

filtering of the regulated 10 volt supply. Diode D1 protects regulator L1 from residual charge on capacitor E2 destroying L1 should the 12 volt input be shorted to ground.

IC regulator L2 (LM317) is configured as a 5 volt regulator. A 12 volt supply is applied to input pin 3. The reference voltage is set by voltage divider resistors R12, R13 while electrolytic capacitor E4 minimizes noise and ensures stability of regulator L2. Electrolytic capacitor E5 provides further filtering of the voltage supply.

Electrolytic capacitors E6 and E1 perform bypass functions and are sited appropriately to prevent current drawn by active circuit elements from generating disturbances on the supply rails.

Finally, it is to be understood that various alterations, modifications and/or additions may be introduced into the constructions and arrangements of parts previously described without departing from the spirit or ambit of the invention.

CLAIMS

1. Apparatus suitable for use with an image storage system, said apparatus including:

at least one image sensor for generating data representing an image applied to said sensor;

means for applying a first image to said at least one sensor for generating first data representing at least relatively coarse features in said first image;

means for applying a second image including an enlarged portion of said first image to said at least one sensor for generating second data representing at least relatively fine features in said first image;

said second data representing said relatively fine features with a set level of definition and said first data representing said relatively coarse features with a level of definition which is below said set level, whereby reducing the quantity of said data for storage purposes.

2. Apparatus according to Claim 1 wherein said at least one image sensor includes a charge coupled device (CCD) array.

3. Apparatus according to claim 1 or 2 wherein said means for applying said first image includes a wide angle lens and said means for applying said second image includes a telephoto lens.

4. Apparatus according to any one of the preceding claims and including processing means for controlling operation of said apparatus.

5. Apparatus according to claim 4 wherein said processing means includes a digital computer having storage means for storing said data.

6. Apparatus according to claim 4 or 5 wherein said processing means includes a frame grabber for freezing said data.

7. Apparatus according to claim 5 or 6 wherein said apparatus is adapted for recording overspeeding vehicles.

8. An image storage system including:

at least one image sensor for generating data representing an image applied to said sensor;

means for applying a first image to said at least

one sensor for generating first data representing at least relatively coarse features in said first image;

means for applying a second image including an enlarged portion of said first image to said at least one sensor for generating second data representing at least relatively fine features in said first image;

said second data representing said relatively fine features with a set level of definition and said first data representing said relatively coarse features with a level of definition which is below said set level; and

means for storing said data.

9. A system according to claim 8 wherein said at least one image sensor includes a charge coupled device (CCD) array.

10. A system according to claim 8 or 9 wherein said means for applying said first image includes a wide angle lens and said means for applying said second image includes a telephoto lens.

11. A system according to any one of claims 8-10 including processing means for controlling operation of said system.

12. Apparatus for recording overspeeding vehicles including an image storage system according to any one of claims 8-11.

13. Apparatus according to claim 12 wherein said apparatus is operable in response to a speed detector.

14. Apparatus substantially as herein described with reference to Figs. 1-4 or Figs. 5-9 of the accompanying drawings.

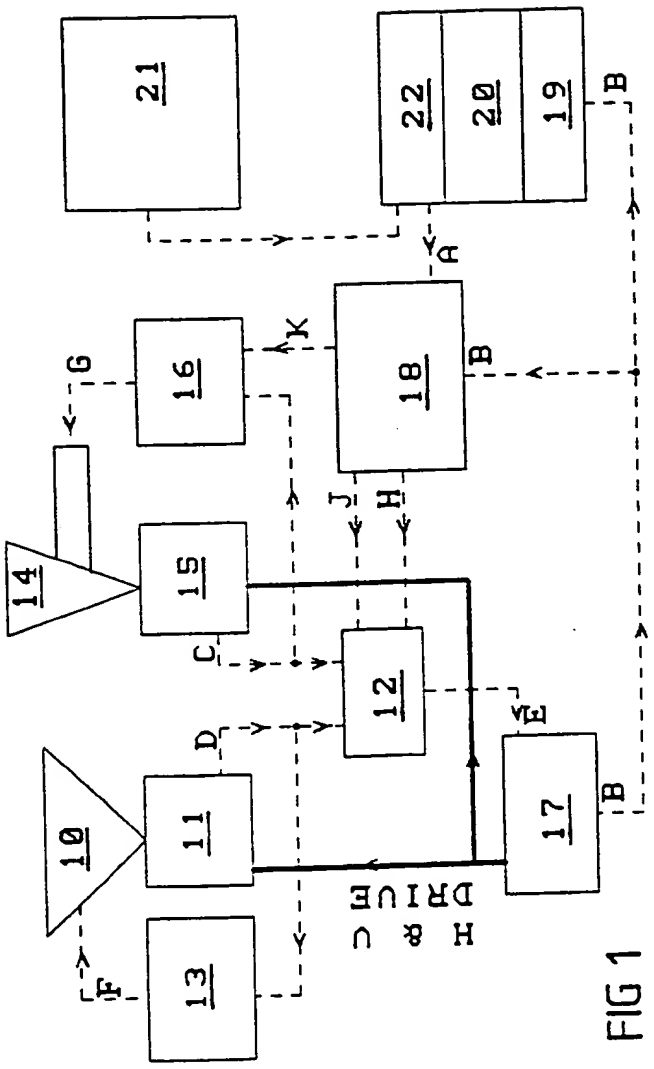


FIG 1

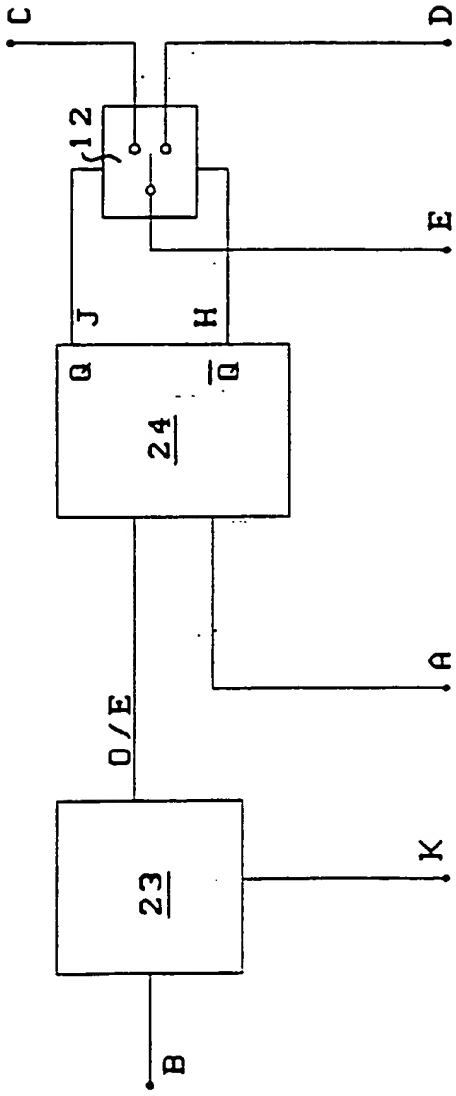


FIG 2

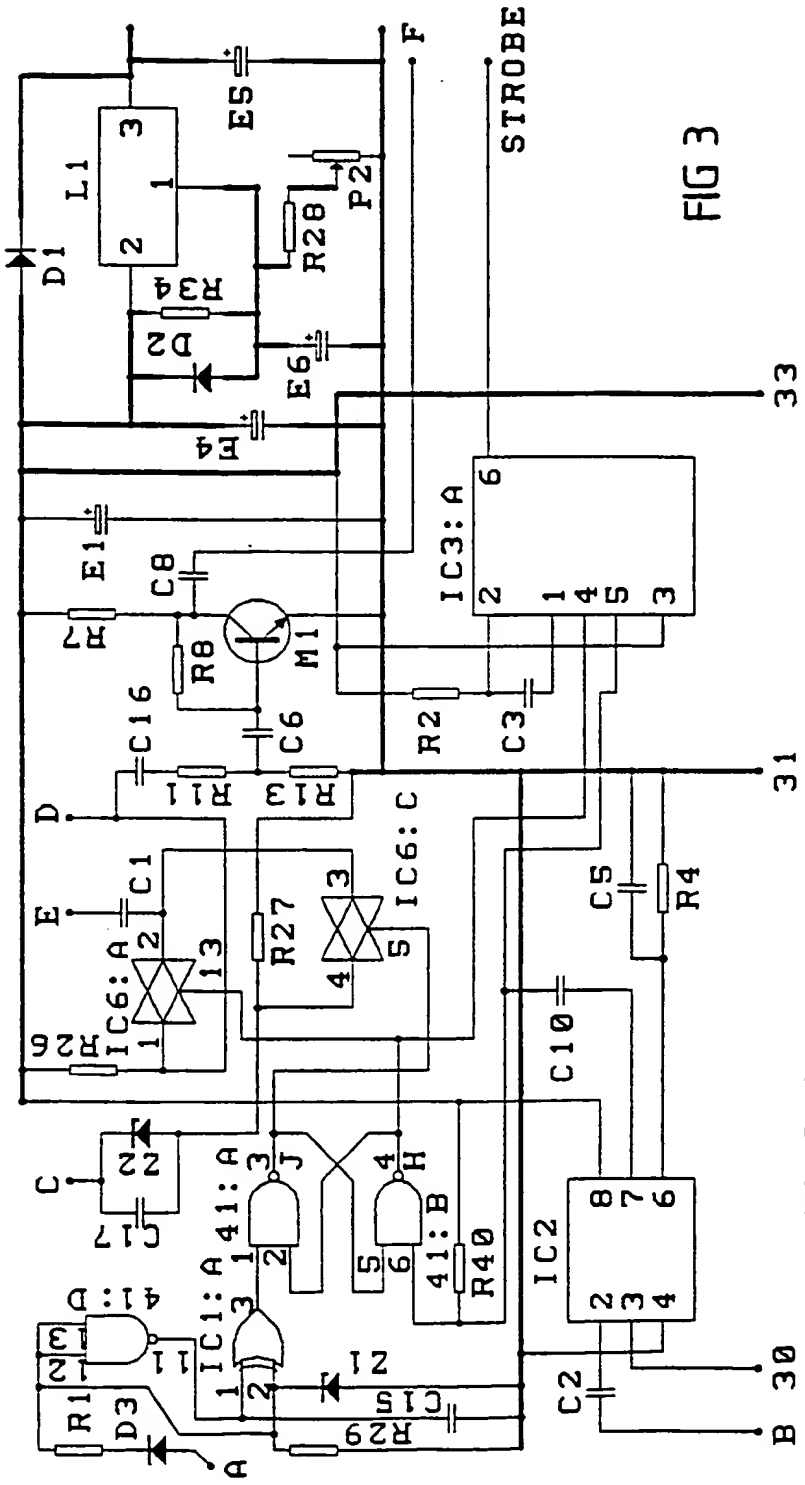

F
STROBE
E5
L1
P2
R28
D1
R34
D2
E6
E4
33
E1
C8
IC3:A
R7
R8
M1
C16
C6
R2
C3
31
D
R11
R13
E
C1
IC6:C
R27
C5
R4
IC6:A
R26
C10
C
IC1:A
IC2
R40
D3
R1
R29
C15
C2
B 30
A
TO FIG 4

FIG 3

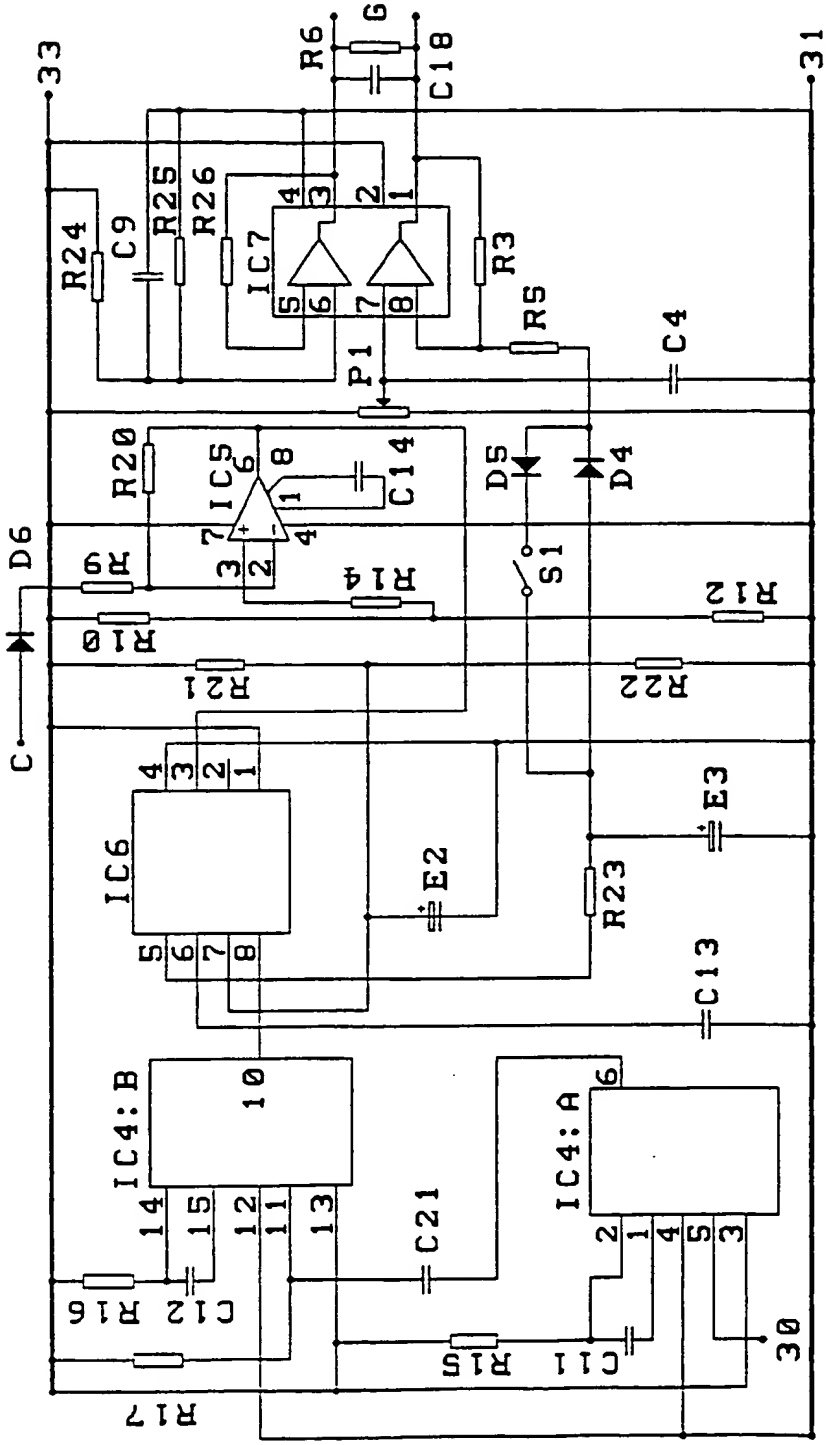
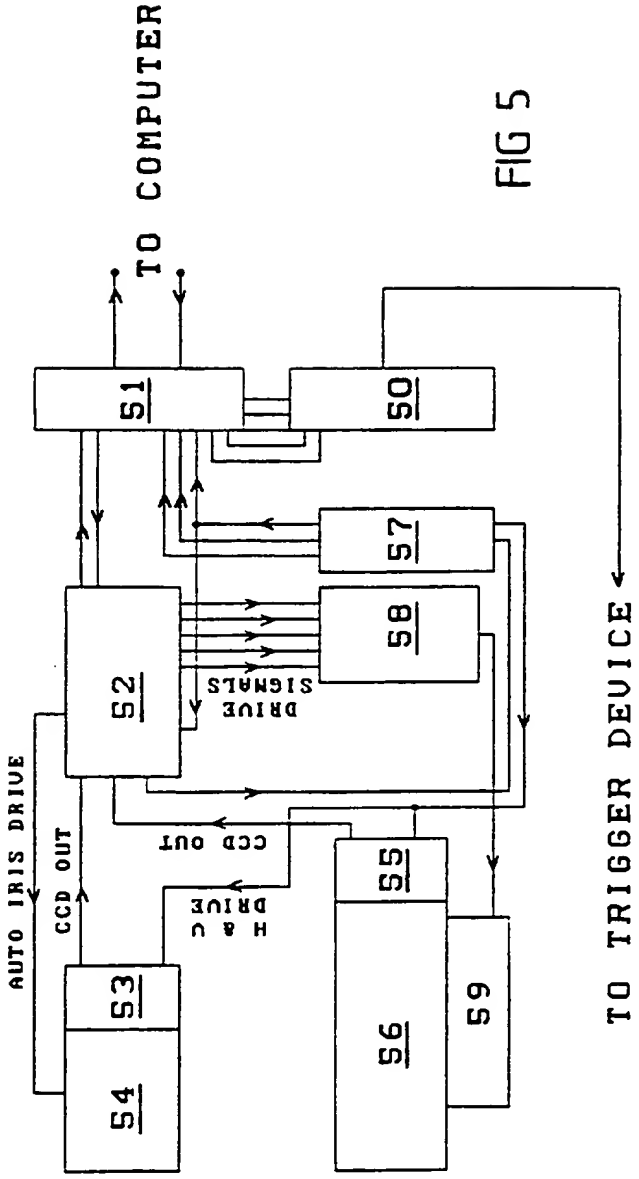

33
31
30
R6
C6
C18
R24
C9
R25
R26
IC7
R3
R5
C4
P1
R20
IC5
C14
D5
D4
D6
R9
R14
S1
R12
R10
R21
R22
C
IC6
E2
E3
R23
C13
IC4:B
IC4:A
C21
C12
R16
R15
C11
R17

FIG 4

FIG 5


TO COMPUTER
51
50
57
58
52
DRIVE SIGNALS
AUTO IRIS DRIVE
CCD OUT
CCD OUT
H & C DRIVE
55
53
54
56
59
TO TRIGGER DEVICE

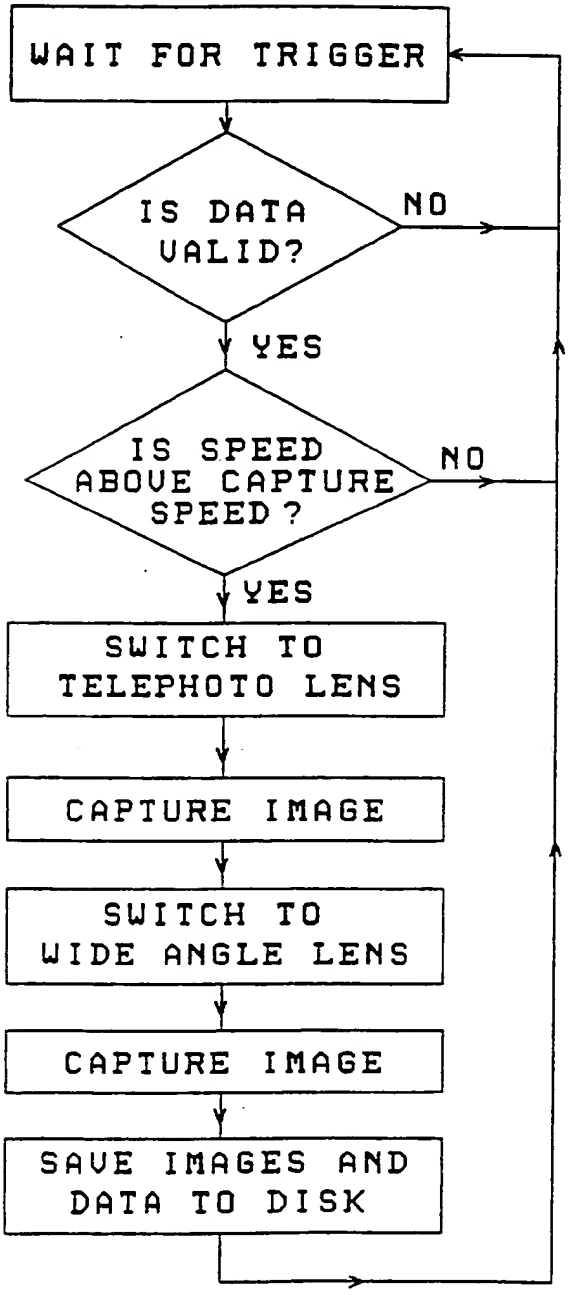
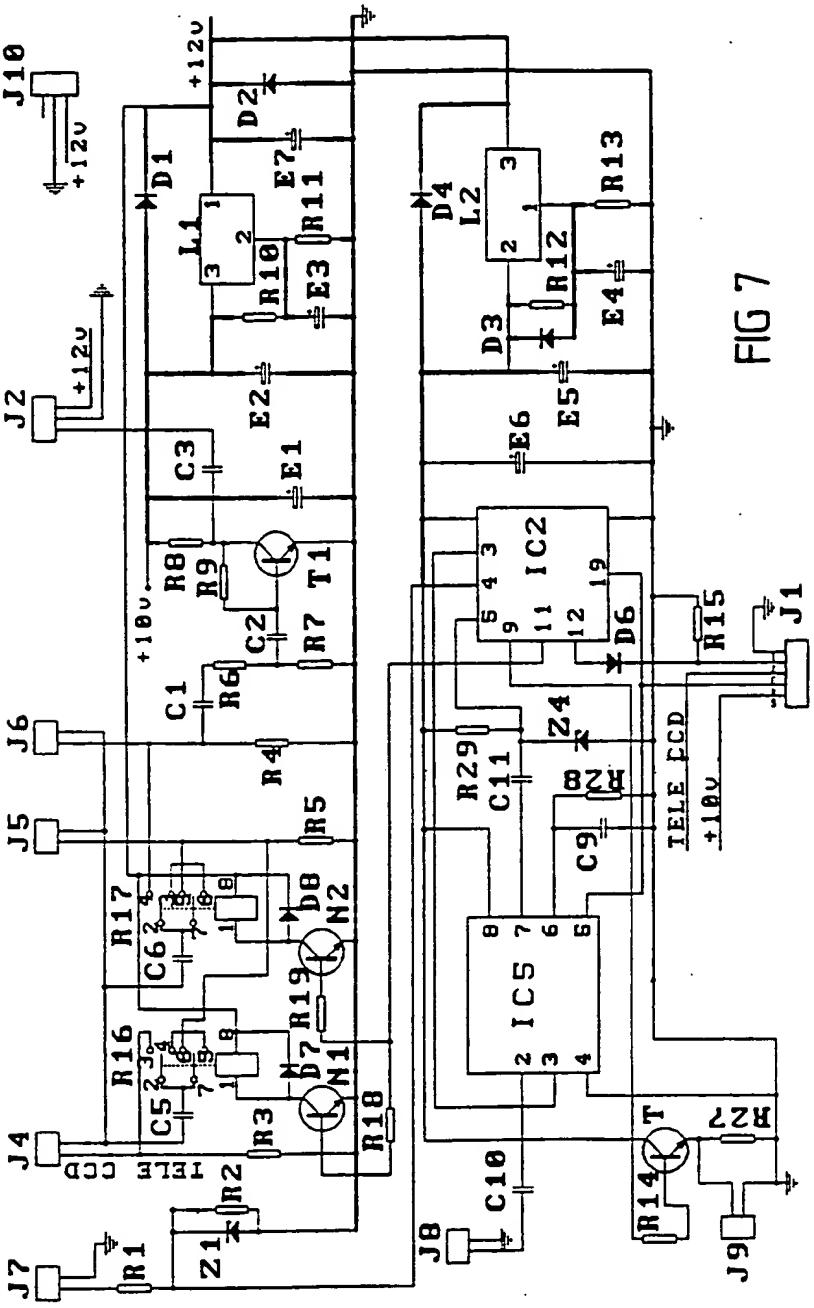

WAIT FOR TRIGGER
IS DATA VALID?
NO
YES
IS SPEED ABOVE CAPTURE SPEED ?
NO
YES
SWITCH TO TELEPHOTO LENS
CAPTURE IMAGE
SWITCH TO WIDE ANGLE LENS
CAPTURE IMAGE
SAVE IMAGES AND DATA TO DISK

FIG 6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+12v
D1
D2
+12v
L1
R10
R11
E3
E7
J2
+12v
C3
E1
E2
R8
R9
T1
+10v
C2
R7
C1
R6
J6
R4
J5
R5
R17
C6
D8
N2
R19
R16
C5
D7
N1
R3
R18
J4
TELE CCD
R2
J7
R1
Z1
D4
L2
R13
R12
E4
D3
E5
E6
IC2
D6
R15
J1
Z4
R29
C11
C9
TELE CCD
+10v
IC5
T
R14
C10
J8
J9

FIG 7

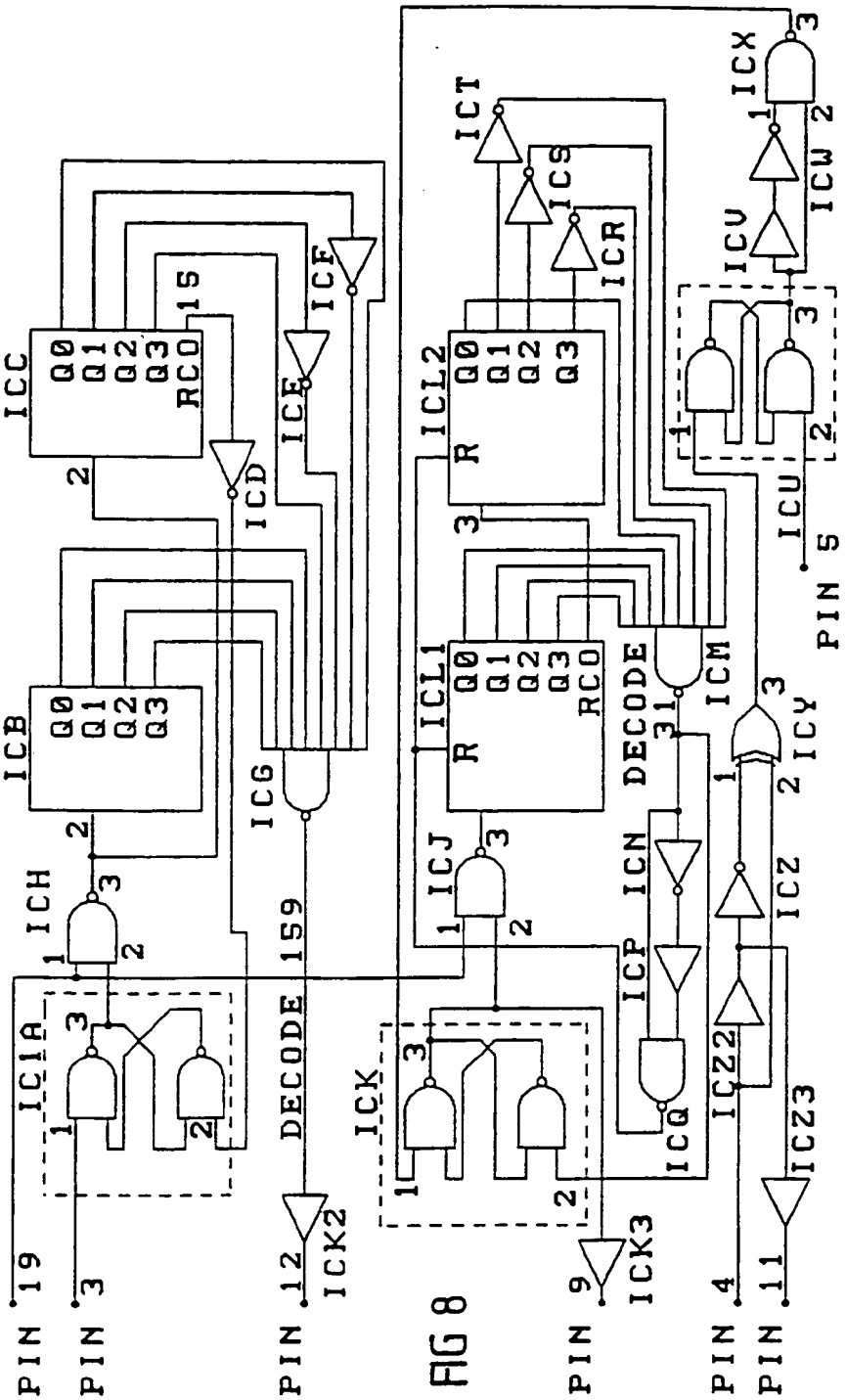
ICC
Q0 Q1 Q2 Q3 RCO
15
ICF
ICE
ICD
ICB
Q0 Q1 Q2 Q3
ICG
ICH
ICIA
DECODE
159
ICK2
PIN 19
PIN 3
PIN 12
ICL2
R
Q0 Q1 Q2 Q3
ICT
ICS
ICR
ICL1
R
Q0 Q1 Q2 Q3 RCO
ICJ
ICK
ICQ
ICP
ICN
DECODE
31
ICM
ICY
ICZ
ICZ2
ICZ3
ICK3
PIN 9
PIN 4
PIN 11
ICX
ICW
ICU
PIN 5

FIG 8

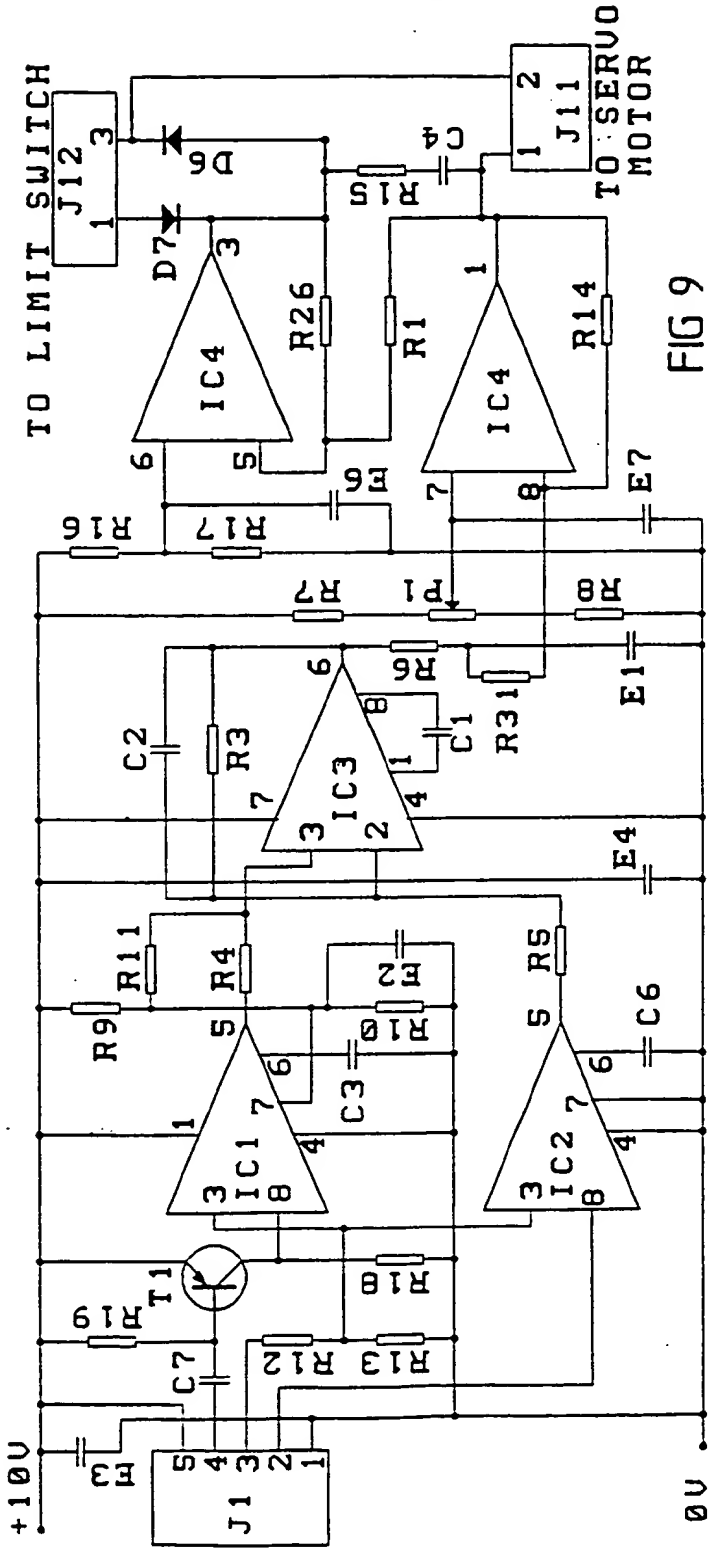
TO LIMIT SWITCH
J12
TO SERVO MOTOR
J11
D6
D7
C4
R15
IC4
R26
R1
R14
R16
R17
R6
E7
R7
P1
R8
E1
C2
R3
IC3
C1
R31
E4
R11
R4
R2
R5
C6
R9
R10
C3
IC1
IC2
T1
R18
R19
R12
R13
C7
E3
J1
+10V
0V

FIG 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU 94/00260

A. CLASSIFICATION OF SUBJECT MATTER
Int. Cl. G08G 1/017, G06K 9/46, 9/36, 9/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC : G08G 1/017, 1/10, G06K 9/46, 9/36, 9/60, G01S 13/92

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
AU : IPC as above

Electronic data base consulted during the international search (name of data base, and where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
X,P	GB,A, 2266398 (TRAFFIC TECHNOLOGY LIMITED) 27 October 1993 (27.10.93) See entire document	1 to 14
X,P	Patent Abstracts of Japan, P1623, page 145, JP,A, 05-151386 (ISHIKAWAJIMA HARIMA HEAVY IND CO LTD (1)) 18 June 1993	1 to 14
A	DE,A, 3535588 (ROBOT FOTO UND ELECTRONIC GmbH & CO KG) 9 April 1987 (09.04.87)	1,2,4,5,8,9, and 11

(continued)

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
18 August 1994 (18.08.94)

Date of mailing of the international search report
26 Aug 1994 (26.08.94)

Name and mailing address of the ISA/AU

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Form PCT/ISA/210 (continuation of first sheet (2)) (July 1992) copjne

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU 94/00260

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate of the relevant passages	Relevant to Claim No.
A	EP,A, 0152355 (NIPPON TELEGRAPH & TELEPHONE PUBLIC CORPORATION) 21 August 1985 (21.08.85)	1,2,4,5,8,9, and 11
A	EP,A, 0132795 (POLAROID CORPORATION) 13 February 1985 (13.02.85)	1,2,4,5,8,9, and 11

INTERNATIONAL SEARCH REPORT

Information on patent family memb

International application No.
PCT/AU 94/00260

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report	Patent Family Member
GB 2266398	AU 39599/93 WO 9321617
JP 151386	NONE
EP 132795	CA 1248218 DE 3485914 EP 132795
DE 3535588	NONE
EP 152355	CA 1234231 DE 3585038 JP 60173623 JP 1008854 US 4742558 JP 60204081 JP 60222972 JP 3019584
	END OF ANNEX